

# MOS FIELD EFFECT TRANSISTOR $\mu$ PA1757

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **Description**

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

#### **Features**

- Dual MOS FET chips in small package
- 2.5 V gate drive type and low on-resistance RDS(on)1 = 23 m $\Omega$  (MAX.) (VGS = 4.5 V, ID = 3.5 A) RDS(on)2 = 32 m $\Omega$  (MAX.) (VGS = 2.5 V, ID = 3.5 A)
- Low Ciss Ciss = 750 pF Typ.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

#### 1; Source 1 2; Gate 1 7, 8; Drain 1 3; Source 2 4; Gate 2 5, 6; Drain 2 6.0 ±0.3 4.4 5.37 Max. 0.8

Package Drawing (Unit: mm)

#### **Ordering information**

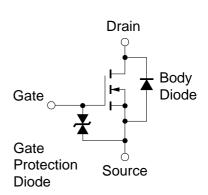
Part Number	Package
μ PA1757G	Power SOP8

#### Absolute Maximum Ratings (T<sub>A</sub> = 25 °C)

Drain to source voltage	VDSS	20	V
Gate to source voltage	Vgss	±12.0	V
Drain current (DC)	I <sub>D(DC)</sub>	±7.0	Α
Drain current (pulse) Note1	D(pulse)	±28	Α
Total power dissipation (1 unit) <sup>Note2</sup>	Рт	1.7	W
Total power dissipation (2 unit) <sup>Note2</sup>	Рт	2.0	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

**Notes 1.** PW  $\leq$  10  $\mu$  s, Duty Cycle  $\leq$  1 %

**2.** T<sub>A</sub> = 25 °C, Mounted on ceramic substrate of 2000 mm<sup>2</sup> x 1.1 mm



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

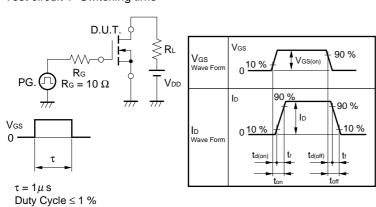
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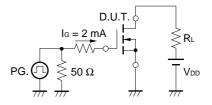
#### Electrical Characteristics (T<sub>A</sub> = 25 °C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to source on-state resistance	RDS(on)1	Vgs = 4.5 V, ID = 3.5 A		16.2	23	mΩ
	RDS(on)2	Vgs = 2.5 V, ID = 3.5 A		22	32	mΩ
Gate to source cutoff voltage	VGS(off)	Vps = 10 V, Ip = 1.0 mA	0.5	0.8	1.5	V
Forward transfer admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.5 A	5.0	13		S
Drain leakage current	Ipss	Vps = 20 V, Vgs = 0 V			10	μΑ
Gate to source leakage current	Igss	Vgs = ±12.0 V, Vps = 0 V			±10	μΑ
Input capacitance	Ciss	Vps = 10 V		750		pF
Output capacitance	Coss	V <sub>GS</sub> = 0 V f = 1 MHz		420		pF
Reverse transfer capacitance	Crss			140		pF
Turn-on delay time	td(on)	ID = 3.5 A		57		ns
Rise time	tr	$V_{GS(on)} = 4.0 \text{ V}$ $V_{DD} = 10 \text{ V}$ $R_G = 10 \Omega$		206		ns
Turn-off delay time	td(off)			593		ns
Fall time	tr			815		ns
Total gate charge	Q <sub>G</sub>	ID = 7.0 A		13.0		nC
Gate to source charge	Qgs	V <sub>DD</sub> = 16 V V <sub>GS</sub> = 4.0 V		2.6		nC
Gate to drain charge	Q <sub>GD</sub>			5.3		nC
Body diode forward voltage	V <sub>F</sub> (S-D)	IF = 7.0 A, Vgs = 0 V		0.75		V

#### Test circuit 1 Switching time

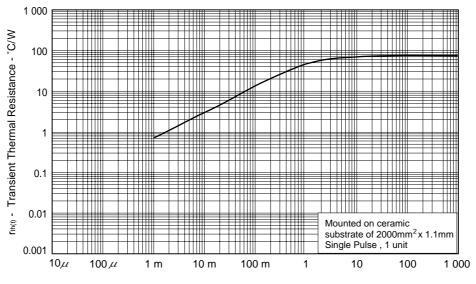


#### Test circuit 2 Gate charge



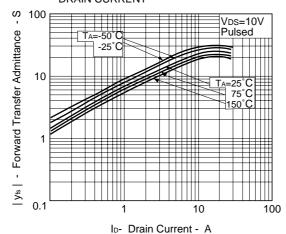
#### Typical Characteristics (T<sub>A</sub> = 25 °C)

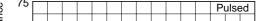
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

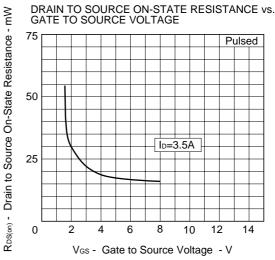


PW - Pulse Width - S

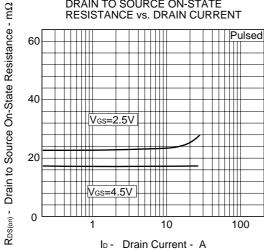
#### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



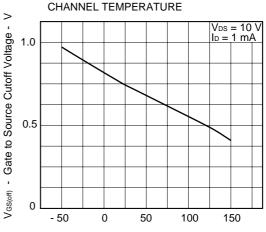




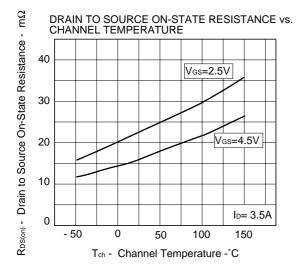
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

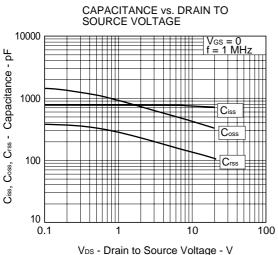


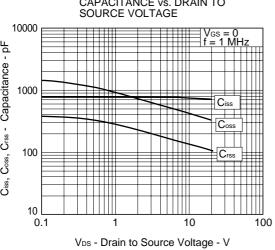
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

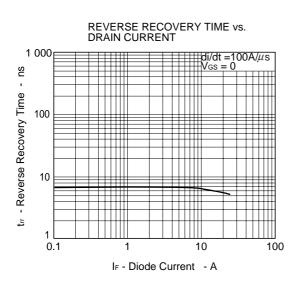


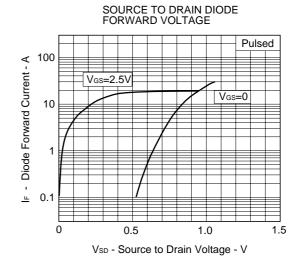
Tch - Channel Temperature -°C

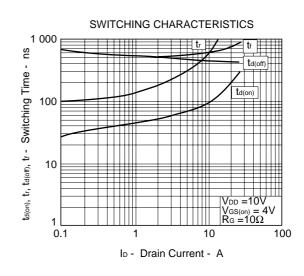


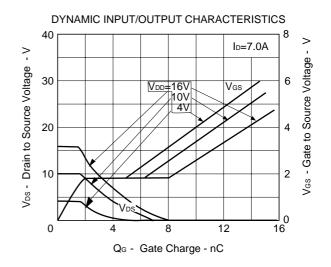


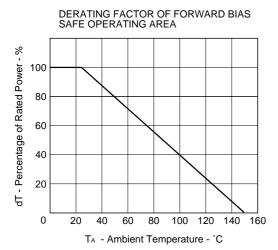




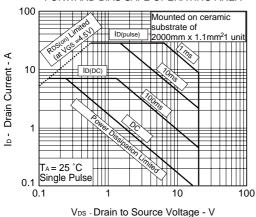




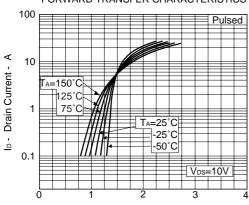




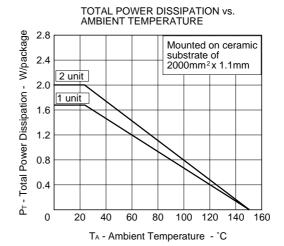
#### FORWARD BIAS SAFE OPERATING AREA



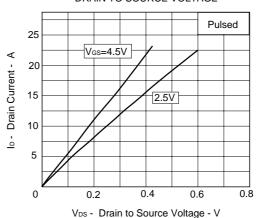
FORWARD TRANSFER CHARACTERISTICS



 $\ensuremath{\mathsf{V}}_\text{GS}\text{-}$  Gate to Source Voltage -  $\ensuremath{\mathsf{V}}$ 



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



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Anti-radioactive design is not implemented in this product.

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